Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) An apparatus for exception handling in a data packet processor, comprising:

a packet processing pipeline including at least two processing stages, each for processing a sequential plurality of data packets, each of said plurality of data packets having an exception map associated therewith, wherein the exception map has one or more entries, each of the entries associated with a particular exception condition;

an exception detector associated with each of said processing stages, said detector detecting whether any of a plurality of exception conditions applies to a data packet; ~~and~~

a bit setter responsive to said exception detector to set, modify, or reset at least one of the entries of an exception map associated with the data packet; and

an exception handler to process said execution map at a stage later than a stage in which said bit setter has set, modified, or reset one of the entries.

2. (Original) The apparatus of claim 1 wherein each of said exception conditions further comprise a plurality of logical operations.

3. (Currently Amended) The apparatus of claim 1 ,wherein said exception handler processes ~~further comprising an exception handler to process~~ said exception map in response to said entries that are set in said exception map when all of said processing stages are complete.

4. (Original) The apparatus of claim 1 further comprising a memory associated with said data packet to store said exception map.

5. (Previously Presented) An apparatus for exception handling in a data packet processor, comprising:

a packet processing pipeline including at least two processing stages, each for processing a sequential plurality of data packets, each of said plurality of data packets having an exception map associated therewith, wherein the exception map has one or more entries, each of the entries associated with a particular exception condition;

an exception detector associated with each of said processing stages, said detector detecting whether any of a plurality of exception conditions applies to a data packet;

a bit setter responsive to said exception detector to set, modify, or reset at least one of the entries of an exception map associated with the data packet; and

an exception handler to further process the data packet in response to said exception map when all of said processing stages are complete.

6. (Original) The apparatus of claim 5 wherein said associated exception condition further comprises a plurality of logical operations.

7. (Original) The apparatus of claim 5 wherein said interpreter further comprises a memory associated with said data packet to store said exception map.

8. (Currently Amended) An apparatus for exception handling in a data packet processor, comprising:

means for processing a sequential plurality of data packets through at least one processing stage, each of said plurality of data packets associated with an exception map, wherein the exception map has one or more entries, each of the entries associated with a particular exception condition;

means for detecting whether any of a plurality of exception conditions applies to said data packet in each processing stage; ~~and~~

means for setting, modifying, or resetting at least one of the entries in said exception map if it is determined that any of said exception conditions applies to said data packets; and

means for processing said exception map at a stage later than a stage in which said bit setter has set, modified, or reset one of the entries.

9. (Original) The apparatus of claim 8 wherein each of said exception conditions further comprise a plurality of logical operations.

10. (Currently Amended) The apparatus of claim 8, wherein said means for processing further comprises ~~further comprising~~ a means for processing said exception map in response to said entries that are set in said exception map when all of said processing stages are complete.

11. (Original) The apparatus of claim 8 further comprising a memory associated with said data packet to store said exception map.

12. (Previously Presented) An apparatus for exception handling in a data packet processor, comprising:

means for processing a sequential plurality of data packets through at least two processing stages, each of said plurality of data packets having an exception map associated therewith, wherein the exception map has one or more entries, each of the entries associated with a particular exception condition;

means for detecting in each of said processing stages whether any of a plurality of exception conditions applies to a data packet;

means for setting, modifying, or resetting at least one of the entries of an exception map associated with said data packet; and

means for processing the data packet in response to said exception map when all of said processing stages are complete.

13. (Original) The apparatus of claim 12 wherein said associated exception condition further comprises a plurality of logical operations.

14. (Original) The apparatus of claim 12 further comprising a means for storing said exception map.

15. (Currently Amended) An apparatus for exception handling in a data packet processor, comprising:

a packet processing pipeline including at least two processing stages for processing a sequential plurality of data packets, each of said plurality of data packets having an exception

map associated therewith, wherein the exception map has one or more entries, each of the entries associated with a particular exception condition;

an exception detector associated with each of said processing stages, said detector detecting, at a stage later than a stage in which an entry has been set, whether any of a plurality of exception conditions applies to a data packet; and

means for setting, modifying, or resetting one or more of the entries of an exception map associated with the data packet.

16. (Original) The apparatus of claim 15 wherein each of said exception conditions further comprise a plurality of logical operations.

17. (Original) The apparatus of claim 15 further comprising a means for processing said exception map in response to said bits that are set in said exception map when all of said processing stages are complete.

18. (Original) The apparatus of claim 15 further comprising a memory associated with said data packet to store said exception map.

19. (Previously Presented) An apparatus for exception handling, comprising:

a packet processing pipeline including at least two processing stages, each for processing a sequential plurality of data packets, each of said plurality of data packets having an exception map associated therewith, wherein the exception map has one or more entries, each of the entries associated with a particular exception condition;

an exception detector associated with each of said processing stages, said detector detecting whether any of a plurality of exception conditions applies to a data packet;

means for setting, modifying, or resetting one or more of the entries of an exception map associated with the data packet; and

means for processing said exception map in response to said exception map when all of said processing stages are complete.

20. (Original) The apparatus of claim 19 wherein each of said exception conditions further comprise a plurality of logical operations.

21. (Original) The apparatus of claim 19 further comprising a memory associated with said data packet to store said exception map.

22. (Currently Amended) A method for exception handling in a data packet processor, comprising:

processing a plurality of data packets through at least two processing stages in said data packet processor, each of said data packets having an exception map associated therewith, wherein the exception map has one or more entries, each of the entries associated with a particular exception condition;

determining whether any of a plurality of associated exception conditions applies to a data packet; ~~and~~

setting, modifying, or resetting one or more of the entries of an exception map associated with the data packet; and

processing said exception map at a stage later than a stage in which said bit setter has set, modified, or reset one of the entries.

23. (Original) The method of claim 22 further comprising applying logical operations to each of said plurality of exception conditions.

24. (Currently Amended) The method of claim 22 wherein said processing further comprises ~~further comprising~~ processing said exception map in response to said entries that are set in said exception map when all of said processing stages are complete.

25. (Original) The method of claim 22 further comprising storing said exception map in a memory associated with said data packet.

26. (Previously Presented) A method for exception handling in a data packet processor, comprising:

processing a plurality of data packets through at least one processing stage in said data packet processor, each of said data packets having an exception map associated therewith, wherein the exception map has one or more entries, each of the entries associated with a particular exception condition;

determining whether any of a plurality of associated exception conditions applies to a data packet;

setting, modifying, or resetting at least one of the entrics of an exception map associated with the data packet; and

processing said associated data packet in response to said exception map when all of said processing stages are complete.

27. (Original) The method of claim 26 further comprising applying logical operations to each of said plurality of exception conditions.

28. (Original) The method of claim 26 further comprising storing said exception map in a memory associated with said data packet.

29. (Currently Amended) A program storage device readable by a machine, tangibly embodying a program of instructions executable by the machine to perform a method for exception handling in a data packet processor, said method comprising:

processing a plurality of data packets through at least two processing stages in said data packet processor, each of said data packets having an exception map associated therewith, wherein the exception map has one or more entries, each of the entries associated with a particular exception condition,

determining whether any of a plurality of associated exception conditions applies to a data packet; ~~and~~

setting, modifying, or resetting one or more entries of an exception map associated with the data packet; and

processing said exception map at a stage later than a stage in which said bit setter has set, modified, or reset one of the entries.

30. (Previously Presented) A program storage device readable by a machine, tangibly embodying a program of instructions executable by the machine to perform a method for exception handling in a data packet processor, said method comprising:

processing a plurality of data packets through at least one processing stage in said data packet processor, each of said data packets having an exception map associated therewith, wherein the exception map has one or more entries, each of the entries associated with a particular exception condition;

determining whether any of a plurality of associated exception conditions applies to a data packet;

setting, modifying, or resetting at least one of the entries of an exception map associated with the data packet; and

processing said associated data packet in response to said exception map when all of said processing stages are complete.

31. (Currently Amended) An apparatus for exception handing in a data packet processor, comprising:

means for processing a plurality of data packets through at least two processing stages in said data packet processor, each of said data packets having an exception map associated therewith, wherein the exception map has one or more entries, each of the entries associated with a particular exception condition;

means for determining whether any of a plurality of associated exception conditions applies to a data packet; ~~and~~

means for setting, modifying, or resetting one or more entries of an exception map associated with the data packet; and

means for processing said exception map at a stage later than a stage in which said bit setter has set, modified, or reset one of the entries.

32. (Original) The apparatus of claim 31 further comprising means for applying logical operations to each of said plurality of exception conditions.

33. (Currently Amended) The apparatus of claim 31, wherein said means for processing further comprises ~~further comprising~~ means for processing said exception map in response to said entries that are set in said exception map when all of said processing stages are complete.

34. (Original) The apparatus of claim 31 further comprising means for storing said exception map in a memory associated with said data packet.

35. (Previously Presented) An apparatus for exception handling in a data packet processor, comprising:

means for processing a plurality of data packets through at least one processing stage in said data packet processor, each of said data packets having an exception map associated therewith, wherein the exception map has one or more entries, each of the entries associated with a particular exception condition;

means for determining whether any of a plurality of associated exception conditions applies to a data packet;

means for setting, modifying, or resetting at least one of the entries of an exception map associated with the data packet; and

means for processing said associated data packet in response to said exception map when all of said processing stages are complete.

36. (Original) The method of claim 35 further comprising means for applying logical operations to each of said plurality of exception conditions.

37. (Original) The method of claim 35 further comprising means for storing said exception map in a memory associated with said data packet.